CLAIMS

What is claimed is:

1. A method comprising:

storing a first signature derived by applying an algorithm to a first bitstream;

receiving a second bitstream; and

altering the second bitstream to generate an altered second bitstream.

2. The method of claim 1, further comprising:

generating a second signature by applying the algorithm to the altered second bitstream, wherein the second signature is identical to the first signature.

3. The method of claim 1, wherein the first bitstream and the second bitstream define respective first and second circuit configurations of a programmable logic device.

4. The method of claim 3, wherein the altered second bitstream defines the second circuit configuration of the programmable logic device.

5. The method of claim 1, wherein the algorithm is a cyclic redundancy check algorithm.

6. The method of claim 1, wherein the first signature is a checksum remainder resulting from dividing the first bitstream by a generator polynomial.

7. The method of claim 1, wherein the altering comprises:

appending a number of digital zero digits to an end of the second bitstream to generate an extended second bitstream;

dividing the extended second bitstream by a generator polynomial to generate an intermediate remainder; and

adding a forcing value to the extended second bitstream, wherein the forcing value equals the intermediate remainder plus the first signature.

8. The method of claim 7, wherein the first signature is generated by dividing the first bitstream by the generator polynomial.

9. The method of claim 7, wherein the dividing is performed using modulo-2 division and wherein the adding a forcing value is performed using modulo-2 addition.

10. The method of claim 1, wherein the altering comprises:

dividing the second bitstream by a generator polynomial to yield a remainder;

comparing a digital value in an Nth bit of the remainder to a digital value in an Nth bit of the first signature; and

adding a logic one to each Nth bit of the second bitstream for which the digital value in the Nth bit of the remainder differs from the value in the Nth bit of the first signature.

11. The method of claim 1, further comprising:

supplying the altered second bitstream to a programmable logic device.

12. A circuit comprising:

a shift register containing exclusive OR gates whose outputs are coupled to flip-flops at register positions that correspond to coefficients of an N-bit generator polynomial, the shift register adapted to receive an extended bitstream one bit at a time;

a bit extender that generates the extended bitstream by appending N bits to a bitstream; and

a hash register that stores an intermediate remainder, wherein the intermediate remainder is the result of dividing the extended bitstream by the generator polynomial.

13. The circuit of claim 12, wherein the bitstream defines a circuit configuration of a programmable logic device.

14. The circuit of claim 12, wherein the dividing of the extended bitstream by the generator polynomial constitutes a cyclic redundancy check algorithm and is performed using modulo-2 division.

15. A circuit comprising:

a digital signature register that stores a first digital signature, wherein the first digital signature is the result of applying a hash function to a first bitstream; and

means for altering a second bitstream to generate an altered second bitstream, wherein a second digital signature is the result of applying the hash function to the altered second bitstream, and wherein the second digital signature is identical to the first digital signature.

16. The circuit of claim 15, wherein the first bitstream and the second bitstream define respective first and second circuit configurations of a programmable logic device.

17. A computer-readable medium having computer-executable instructions for performing steps comprising:

storing a first signature derived by applying an algorithm to a first bitstream;

receiving a second bitstream; and

altering the second bitstream to generate an altered second bitstream.

18. The computer-readable medium of claim 17 having further computer-executable instructions for performing the steps of:

supplying the altered second bitstream to a programmable logic device.

19. The computer-readable medium of claim 17 having further computer-executable instructions for performing the steps of:

generating a second signature by applying the algorithm to the altered second bitstream, wherein the second signature is identical to the first signature.

20. A computer-readable medium having stored thereon a data structure generated by executing the steps comprising:

storing a first signature derived by applying an algorithm to a first bitstream;

receiving a second bitstream;

appending a number of digital zero digits to an end of the second bitstream to generate an extended second bitstream;

dividing the extended second bitstream by a generator polynomial to generate an intermediate remainder;

adding the intermediate remainder to the first signature to generate a forcing value; and

adding the forcing value to the extended second bitstream to obtain an altered bitstream.

21. The computer-readable medium of claim 20, wherein the altered bitstream defines a circuit configuration of a field programmable gate array.

22. The computer-readable medium of claim 20, wherein the dividing is performed using modulo-2 division.